WHAT IS CLAIMED IS:

1. A process for forming at least one portion of a compound material formed from elements of an initial material and of a metal within an electronic circuit, comprising the following steps:

(a) formation of a cavity that includes at least one opening onto an access surface and has an internal wall having at least one region of initial material;

(b) deposition of the metal close to said region of initial material;

(c) heating of the circuit so as to form a portion of compound material in said region of initial material; and

(d) removal of at least one portion of the metal that has not formed some of the compound material from the cavity via said opening.

2. The process according to Claim 1, wherein step (a) comprises the removal of at least one material from the circuit.

3. The process according to Claim 1, wherein step (a) comprises the transfer of at least one material from

a temporary substrate to a final substrate carrying the electronic circuit.

4. The process according to Claim 1, wherein the initial material comprises silicon, germanium, arsenic, selenium, or a mixed compound comprising at least one of the above elements.

5. The process according to Claim 1, wherein step (b) comprises introducing the metal into the cavity via the opening so as to form a deposition of the metal on at least said region of initial material.

6. The process according to Claim 1, wherein step (b) comprises depositing the metal outside the cavity close to said opening and wherein, during step (c), the metal diffuses into the cavity, via said opening of the cavity, as far as said region of initial material, so as to form a portion of the compound material in said region of initial material.

7. The process according to Claim 1, wherein step (b) comprises a chemical deposition of the metal from gaseous precursor compounds incorporating atoms of the metal, or a deposition using a liquid solution introduced into the cavity and incorporating dissolved chemical compounds based on the metal in an oxidized form.

8. The process according to Claim 1, wherein the metal comprises cobalt, tantalum, tungsten, titanium, aluminium, copper, silver, platinum, nickel or an alloy comprising at least one of the above metals.

9. The process according to Claim 1, wherein the compound material formed is electrically conducting.

10. The process according to Claim 1, wherein step (d) comprises an etching by means of a solution including chemical reactants.

11. The process according to Claim 1, wherein, during step (c), substantially all the initial material present

in said region of initial material is converted into compound material.

12. The process according to Claim 1, wherein the internal wall of the cavity has at least two regions of initial material separated by an intermediate region of a material other than the initial material and wherein, during step (c), the initial material of at least one of said regions of initial material is made to diffuse into the metal so as to form a portion of compound material connecting said regions of initial material.

13. The process according to Claim 1, wherein the internal wall of the cavity has a region of silica or of silicon nitride.

14. The process according to Claim 1, wherein the cavity comprises a cylindrical or parallelepipedal first volume open to the access surface.

15. The process according to Claim 14, wherein the cavity furthermore comprises a second volume into which the

first volume runs on the opposite side from the access surface, the second volume extending further than the first volume parallel to the access surface.

16. An electronic circuit including a portion of compound material manufactured by the process of Claim 1.

17. The electronic circuit according to Claim 16, wherein the portion of compound material comprises at least one electrical connection.

18. An MOS transistor including a gate having a portion of compound material manufactured by the process of Claim 1.

19. The MOS transistor according to Claim 18, wherein the compound material has a work function within a range of ±25% around a mean value of two work functions of a p-type semiconductor material and an n-type semiconductor material, respectively.

20. An electronic circuit including an MOS transistor having a gate with a portion of compound material manufactured by the processing of Claim 18.

21. A process for MOS transistor gate formation, comprising the steps of:

depositing a temporary material;

forming a transverse structure including a silicon bar doped to define source, drain and channel regions;

removing the temporary material from under the transverse structure to define a cavity;

depositing a metal on exposed surfaces of the transverse structure and in the cavity; and

heating to convert the portions of the silicon bar adjacent to deposited metal into silicide.

22. The method of claim 21 further including removing the deposited metal which is not converted to silicide by heating.

23. The method of claim 21 wherein heating converts certain portions of the silicon bar to define source and drain electrical contacts of the transistor.

24. The method of claim 21 wherein heating converts certain portions of the silicon bar to define a gate surrounding the channel region.

25. The MOS transistor formed by using the method of claim 21.

26. A process for producing electrical connections between separate circuit portions, comprising:

defining first and second separate silicon portions;

depositing a metal overlying the first and second separate silicon portions and a structure therebetween; and

heating to convert portions of the first and second silicon portions adjacent to deposited metal into silicide, wherein the silicide from the first and second silicon portions connects.

27. The process of claim 26 wherein the first and second separate silicon portions may be vertically separated.

28. The process of claim 26 wherein the first and second separate silicon portions may be horizontally separated.

29. The process of claim 26 further including:

forming a temporary material adjacent the first and second separate silicon portions;

burying the temporary material and first and second separate silicon portions with a covering material;

forming a chimney through the covering material to reach the temporary material; and

removing the temporary material through the chimney to form a cavity.

30. The process of claim 29 wherein depositing comprises depositing the metal through the chimney to at least partially fill the cavity.

31. The method of claim 26 further including removing the deposited metal which is not converted to silicide by heating.

32. The electrical connection formed by using the method of claim 26.